

WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:
  - a memory cell array in which memory cells are arranged in a matrix;
  - 5 a plurality of word lines connecting gate terminals of memory cells commonly in a row direction;
  - a plurality of bit lines connecting drain terminals of memory cells commonly in a column direction;
  - a determination circuit for determining data of the memory cells;
  - 10 a column selection circuit for selectively connecting the bit lines to the determination circuit;
  - a charging circuit for charging the bit line selected by the column selection circuit and an input terminal of the determination circuit; and
  - a charge signal generation circuit for controlling the charging circuit,
  - 15 wherein the charging circuit includes:
    - a first charging subcircuit that is operated when an output signal of the charge signal generation circuit is in an active state; and
    - a second charging subcircuit that is operated when the output signal of the charge signal generation circuit is in an active state and a voltage of
    - 20 the selected bit line is lower than a predetermined voltage.
2. A semiconductor memory device, comprising:
  - a memory cell array in which memory cells are arranged in a matrix;
  - a plurality of word lines connecting gate terminals of memory cells
  - 25 commonly in a row direction;
  - a plurality of bit lines connecting drain terminals of memory cells commonly in a column direction;
  - a determination circuit for determining data of the memory cells;
  - a column selection circuit for selectively connecting the bit lines to the
  - 30 determination circuit;
  - a charging circuit for charging the bit line selected by the column selection circuit and an input terminal of the determination circuit; and
  - a charge signal generation circuit for controlling the charging circuit,
  - wherein the charging circuit includes:
  - 35 a first transistor having a source terminal supplied with a supply voltage, a gate terminal supplied with an output signal of the charge signal generation circuit, and a drain terminal connected to an input terminal of the

determination circuit;

a second transistor having a source terminal supplied with the supply voltage and a gate terminal supplied with the output signal of the charge signal generation circuit; and

5 a third transistor having a source terminal connected to a drain terminal of the second transistor, a gate terminal connected to the output terminal of the determination circuit, and a drain terminal connected to the input terminal of the determination circuit.

10 3. A semiconductor memory device, comprising:

a memory cell array in which memory cells are arranged in a matrix;  
a plurality of word lines connecting gate terminals of memory cells  
commonly in a row direction;

15 a plurality of bit lines connecting drain terminals of memory cells  
commonly in a column direction;

a determination circuit for determining data of the memory cells;  
a column selection circuit for selectively connecting the bit lines to the  
determination circuit;

20 a charging circuit for charging the bit line selected by the column  
selection circuit and an input terminal of the determination circuit; and  
a charge signal generation circuit for controlling the charging circuit,  
wherein the charging circuit includes:

25 a first transistor having a source terminal supplied with a supply  
voltage, a gate terminal supplied with an output signal of the charge signal  
generation circuit, and a drain terminal connected to an input terminal of the  
determination circuit;

a second transistor having a source terminal supplied with the supply  
voltage and a gate terminal supplied with the output signal of the charge  
signal generation circuit;

30 a third transistor having a source terminal connected to a drain  
terminal of the second transistor and a drain terminal connected to the input  
terminal of the determination circuit; and

35 an inverter having an input terminal connected to the input terminal  
of the determination circuit and an output terminal connected to a gate  
terminal of the third transistor.

4. A semiconductor memory device, comprising:

a memory cell array in which memory cells are arranged in a matrix;  
 a plurality of word lines connecting gate terminals of memory cells  
 commonly in a row direction;  
 a plurality of bit lines connecting drain terminals of memory cells  
 5 commonly in a column direction;  
 a determination circuit for determining data of the memory cells;  
 a column selection circuit for selectively connecting the bit lines to the  
 determination circuit;  
 a charging circuit for charging the bit line selected by the column  
 10 selection circuit and an input terminal of the determination circuit; and  
 a first charge signal generation circuit for controlling the charging  
 circuit,  
 the device further comprising:  
 a dummy memory cell array in which dummy memory cells are  
 15 arranged in a column direction;  
 a dummy bit line connecting drain terminals of the dummy memory  
 cells;  
 a dummy determination circuit;  
 a dummy selection circuit for connecting the dummy bit line to the  
 20 dummy determination circuit;  
 a dummy charging circuit having the same internal configuration as  
 that of the charging circuit, for receiving an output signal of the first charge  
 signal generation circuit and charging the dummy bit line connected through  
 the dummy selection circuit and an input terminal of the dummy  
 25 determination circuit; and  
 a second charge signal generation circuit for receiving an output  
 signal of the dummy determination circuit and an output signal of the first  
 charge signal generation circuit to control the charging circuit,  
 wherein the charging circuit includes:  
 30 a first charging subcircuit that is operated when the output signal of  
 the first charge signal generation circuit is in an active state; and  
 a second charging subcircuit that is operated when the output signal  
 of the first charge signal generation circuit is in an active state and the  
 output signal of the dummy determination circuit is in a predetermined logic  
 35 state.

5. A semiconductor memory device, comprising:

a memory cell array in which memory cells are arranged in a matrix;  
 a plurality of word lines connecting gate terminals of memory cells  
 commonly in a row direction;  
 a plurality of bit lines connecting drain terminals of memory cells  
 5 commonly in a column direction;  
 a determination circuit for determining data of the memory cells;  
 a column selection circuit for selectively connecting the bit lines to the  
 determination circuit;  
 a charging circuit for charging the bit line selected by the column  
 10 selection circuit and an input terminal of the determination circuit; and  
 a first charge signal generation circuit for controlling the charging  
 circuit,  
 the device further comprising:  
 a dummy memory cell array in which dummy memory cells are  
 15 arranged in a column direction;  
 a dummy bit line connecting drain terminals of the dummy memory  
 cells;  
 a dummy determination circuit;  
 a dummy selection circuit for connecting the dummy bit line to the  
 20 dummy determination circuit;  
 a dummy charging circuit having the same internal configuration as  
 that of the charging circuit, for receiving an output signal of the first charge  
 signal generation circuit and charging the dummy bit line connected through  
 the dummy selection circuit and an input terminal of the dummy  
 25 determination circuit; and  
 a second charge signal generation circuit for receiving an output  
 signal of the dummy determination circuit and the output signal of the first  
 charge signal generation circuit to control the charging circuit,  
 wherein the charging circuit includes:  
 30 a first transistor having a source terminal supplied with a supply  
 voltage, a gate terminal supplied with the output signal of the first charge  
 signal generation circuit, and a drain terminal connected to the input  
 terminal of the determination circuit; and  
 a second transistor having a source terminal supplied with the supply  
 35 voltage, a gate terminal supplied with an output signal of the second charge  
 signal generation circuit, and a drain terminal connected to the input  
 terminal of the determination circuit.